AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

Claims 1-31 (Canceled).

32. (Currently amended) An integrated circuit comprising:

a reflective layer having a reflective upper surface defining a first interface;

a first anti-reflective coating layer formed over the reflective ~~surface~~ layer, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a [[first]] second interface;

a second anti-reflective coating layer formed over ~~and in contact with~~ said first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a ~~second~~ third interface, wherein the first, second, and third interface reflects radiation, and wherein ~~first index of refraction is different from the second index of refraction and~~ the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coating layers are [[chosen]] such that the amplitudes are approximately equal and the phase differences ~~of all sources~~ of the reflected radiation from said first, second, and third interfaces ~~which reside at or below the second interface~~ substantially mutually cancel when combined.

Claims 33-35 (Canceled).

36. (Previously Presented) The integrated circuit according to claim 32, further comprising at least one additional anti-reflective coating layer formed over the first and second anti-reflective coating layers.

37. (Currently amended) The integrated circuit according to claim 32, further comprising a dielectric material formed over the second anti-reflective coating layer.

38. (Previously presented) The integrated circuit according to claim 32, wherein the thickness of the first anti-reflective coating layer is approximately 40 nanometers and the thickness of the second anti-reflective coating layer is approximately 25 nanometers.

39. (Original) The integrated circuit according to claim 32, wherein the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

40. (Currently amended) A memory cell comprising:

a structure on a substrate, the structure comprising:

at least two active areas formed in the substrate;

a gate stack between the active areas;

a capacitor electrically coupled with one of the active areas;

a first anti-reflective coating layer formed over the structure, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface;

a second anti-reflective coating layer formed on at least a portion of the first anti-reflective coating layer, the second anti-reflective coating layer having a second

index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface; and

an insulating layer formed over the second anti-reflective coating layer, wherein the first index of refraction is different from the second index of refraction, wherein the first and second interface reflects radiation, and wherein the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coating layers are such that the amplitudes are approximately equal and the phase differences of the reflected radiation from said first and second interfaces substantially mutually cancel when combined.

41. (Canceled).

42. (Previously presented) The memory cell according to claim 40, wherein the second anti-reflective coating layer is formed entirely on said first anti-reflective coating layer.

43. (Canceled).

44. (Previously presented) The memory cell according to claim 40, wherein the structure is a dual DRAM cell structure comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical communication with the first active area, the second capacitor being in electrical communication with the third active area, and the second active area being in electrical communication with a bit line.

45. (Original) The memory cell according to claim 44, wherein the capacitors are formed over the gate stacks.

46. (Original) The memory cell according to claim 45, wherein the capacitors are container capacitors.

47. (Original) The memory cell according to claim 44, wherein the bit line is formed over the capacitors.

48. (Previously presented) The memory cell according to claim 40, wherein the thickness of the first anti-reflective coating layer is approximately 40 nanometers and the thickness of the second anti-reflective coating layer is approximately 25 nanometers.

49. (Canceled).

50. (Currently amended) An integrated circuit comprising:

at least one memory cell, the memory cell comprising:

a structure on a substrate, the structure comprising:

at least two active areas formed in the substrate;

a gate stack between the active areas;

a capacitor in electrical contact with one of the active areas;

an etch stop layer comprising:

a first anti-reflective coating layer formed over the structure, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness and an upper surface defining a first interface;

a second anti-reflective coating layer formed over and in contact with at least a portion of the first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness and an upper surface defining a second interface, wherein the first and second interface reflects radiation, and wherein ~~first index of refraction is different from the second index of refraction and~~ the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coating layers are [[chosen]] such that the amplitudes are approximately equal and the phase differences ~~of all sources~~ of the reflected radiation from said first and second interfaces ~~which reside at or below the second interface~~ substantially mutually cancel when combined; and

an insulating layer formed over the structure.

51. (Currently amended) A computer system comprising:

a processor; and

a memory, the memory comprising at least one memory cell, the memory cell comprising:

a structure on a substrate, the structure comprising:

at least two active areas formed in the substrate;

a gate stack between the active areas;

a capacitor in electrical contact with one of the active areas;

a first anti-reflective coating layer formed over the structure, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, an upper surface defining a first interface; and

a second anti-reflective coating layer formed in contact with the first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness, an upper surface defining a second interface, wherein the first and second interface reflects radiation, and wherein ~~first index of refraction is different from the second index of refraction and~~ the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coating layers are [[chosen]] such that the amplitudes are approximately equal and the phase differences ~~of all sources~~ of the reflected radiation from said first and second interfaces ~~which reside at or below the second interface~~ substantially mutually cancel when combined.

Claims 52-58 (Canceled).

59. (Previously presented) The integrated circuit according to claim 32, further comprising an inter-level dielectric layer located below said first and second anti-reflective coating layers.

60. (Previously presented) An integrated circuit comprising:

a reflective layer having a reflective surface;

a first silicon dioxide layer formed over the reflective layer;

a first anti-reflective coating layer formed over and in contact with the first silicon dioxide layer, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface, wherein the first reflective coating layer is on the first silicon dioxide layer;

a second anti-reflective coating layer in contact with said first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction; and

a second silicon dioxide layer formed over the second anti-reflective coating layer.

61. (Currently amended) An integrated circuit comprising:

a reflective layer having a reflective surface; and

an etch-stop layer comprising:

a first anti-reflective coating layer formed over the reflective surface, the first anti-reflective coating layer having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface; and

a second anti-reflective coating layer in contact with said first anti-reflective coating layer, the second anti-reflective coating layer having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction and the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coating layers are [[chosen]] such that the amplitudes <u>of all</u>

sources of reflected radiation are approximately equal and the phase differences of ~~all sources of~~ said reflected radiation ~~which reside at or below the second interface substantially mutually cancel when combined~~ is approximately 180° out of phase.

62. (Canceled).

63. (New) An integrated circuit comprising:

a reflective layer having a reflective surface; and

an etch stop layer formed over said reflective layer consisting of:

a first anti-reflective coating layer having an upper surface defining a first interface; and

a second anti-reflective coating layer having an upper surface defining a second interface, wherein the reflective layer, first interface, and second interface reflects radiation, and wherein the first and second anti-reflective coating layers are formed such that the amplitudes and phase differences from said reflected radiation substantially cancel when combined at or below said second interface.